Mackly Monestime

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L1          121 S (STANDARD? OR FORMAL) (2A) FORMAT?  (5A) COMPRES? (2A) (IMAGE
L2            0 S L1 (P) (RECONFIGU? OR CONFIGUR? OR PROGRAM?) (P) SECOND FORMA
L3           13 S L1 (P) (RECONFIGU? OR CONFIGUR? OR PROGRAM?)
L4           11 S FIRST STAND? FORMAT? (P) SECOND STAND? FORMAT?
L5          326 S FIRST (2A) FORMAT? (P) SECOND (2A) FORMAT?  (P) (RECONFIGUR?
L6            2 S L5 (P) DECOD? (3A) DATA (2A) (IMAGE OR VIDEO)
L7            3 S L5 (P) COMPRES? (3A) (IMAGE OR DATA)  (P) DECOD?
L8            2 S L7 NOT L6
L9            8 S L5 (P) COMPRES? (3A) (IMAGE OR DATA)
L10           0 S L3 AND L5
L11        4753 S FIRST (2A) FORMAT? (P) SECOND (2A) FORMAT?
L12          12 S L11 (P) COMPRES? (3A) (IMAGE OR DATA)  (P) DECOD?

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L4 ANSWER 3 OF 11 USPATFULL
PI US 5477228 19951219
AB Differential correction signals for a global positioning system (GPS), which operates with signals from a plurality of orbiting satellites, are provided in a **first standard format**, such as a RTCM SC-104 format, for each satellite in view of a reference receiver station. The differential correction signals include range error correction signals and range rate error correction information. The differential correction signals are then encoded according to a **second standard format**, such as the RDS format. The transmission time of the signals in the **second standard format** are then prioritized. A broadcast transmitter, such as a broadcast FM transmitter, is then modulated by the prioritized signals in the **second standard format** and a receiver receives and demodulates the broadcast signal. The broadcast prioritized signals in the **second standard format** are then decoded to provide differential correction signals in the **first standard format**. Various prioritization schemes are provided such as: prioritizing according to the maximum range acceleration rate for the various satellites; prioritizing according to the range acceleration rate for the various satellites exceeding a predetermined absolute value; prioritizing according to range error correction signals exceeding a predetermined absolute value; and prioritizing according to the range error or acceleration corrections signals for the various satellites. In addition to prioritizing, the RTCM signals is compressed and a 1/8 minute time clock is used to simplify processing at a user receiver.

SUMM In accordance with this and other objects of the invention, a system provides differential correction signals for a global positioning system (GPS) which operates with signals from a plurality of orbiting satellites. Differential correction signals are provided in a **first standard format**, such as a RTCM SC-104 format, for each satellite in view of a reference receiver station. The differential correction signals in the **first standard format** are then encoded according to a **second standard format**, such as the RDS format. The transmission time of the signals in the **second standard format** are then prioritized. A broadcast transmitter, such as a broadcast FM transmitter, is then modulated by the prioritized signals in the **second standard format**. A receiver receives and demodulates the broadcast signal. The broadcast prioritized signals in the **second standard format** are then decoded to provide differential correction signals in the **first standard format**.

CLM What is claimed is:
1. A system for broadcasting differential correction signals for a global positioning system (GPS) which includes a plurality of orbiting satellites, comprising: means for providing differential correction signals in a **first standard format** for various ones of a plurality of satellites; means for converting said differential corrections signals in the **first standard format** to signals in a **second standard format**; means for prioritizing the broadcast transmission time of the signals in the **second standard format** ; transmitter means for broadcasting a signal modulated by the prioritized signals in the **second standard**

format; receiver means for receiving and demodulating the broadcast signal modulated by the prioritized signals in the **second standard format**; means for reconverting the broadcast prioritized signals in the **second standard format** to provide differential correction signals in the **first standard format**.

10. A system for broadcast transmitting differential correction signals for global positioning system GPS which includes a plurality of orbiting satellites, comprising: means for providing differential correction signals in a **first standard format** for various ones of a plurality of satellites; means for converting said differential corrections signals in the **first standard format** to guide in a **second standard format**; means for prioritizing the transmission time of the signals in the **second standard format**; transmission means for broadcasting a signal modulated by the prioritized signals in the **second standard format**.

24. A system for broadcasting differential correction signals for a global positioning system (GPS) which includes a plurality of orbiting satellites, comprising: means for providing differential correction signals in a **first standard format** for various ones of a plurality of satellites, wherein the differential correction signals include range error correction signals and range rate error correction information; means for converting said differential correction signals in the **first standard format** to signals in a **second standard format**; means for prioritizing the broadcast transmission time of the signals in the **second standard format** , wherein the means for prioritizing the transmission time of the signals in the **second standard format** includes means for prioritizing according to the maximum range acceleration rate for the various satellites; transmitter means for broadcasting a signal modulated by the prioritized signals in the **second standard format**; receiver means for receiving and demodulating the broadcast signal modulated by the prioritized signals in the **second standard format**; means for reconverting the broadcast prioritized signals in the **second standard format** to provide differential correction signals in the **first standard format**.

25. A system for broadcasting differential correction signals for a global positioning system (GPS) which includes a plurality of orbiting satellites, comprising: means for providing differential correction signals in a **first standard format** for various ones of a plurality of satellites, wherein the differential correction signals include range error correction signals and range rate error correction information; means for converting said differential correction signals in the **first standard format** to signals in a **second standard format**; means for prioritizing the broadcast transmission time of the signals in the **second standard format** , wherein the means for prioritizing the transmission time of the signals in the **second standard format** includes means for prioritizing according to the range acceleration rate for the various satellites exceeding a predetermined absolute value; transmitter means for broadcasting a signal modulated by the prioritized

signals in the **second standard format;**
receiver means for receiving and demodulating the broadcast signal modulated by the prioritized signals in the **second standard format;** means for reconverting the broadcast prioritized signals in the **second standard format** to provide differential correction signals in the **first standard format.**

26. A system for broadcasting differential correction signals for a global positioning system (GPS) which includes a plurality of orbiting satellites, comprising: means for providing differential correction signals in a **first standard format** for various ones of a plurality of satellites, wherein the differential correction signals include range error correction signals and range rate error correction information; means for converting said differential correction signals in the **first standard format** to signals in a **second standard format;** means for prioritizing the broadcast transmission time of the signals in the **second standard format** , wherein the means for prioritizing the transmission time of the signals in the **second standard format** includes means for prioritizing according to range error correction signals exceeding a predetermined absolute value; transmitter means for broadcasting a signal modulated by the prioritized signals in the **second standard format;** receiver means for receiving and demodulating the broadcast signal modulated by the prioritized signals in the **second standard format;** means for reconverting the broadcast prioritized signals in the **second standard format** to provide differential correction signals in the **first standard format.**

27. A system for broadcasting differential correction signals for a global positioning system (GPS) which includes a plurality of orbiting satellites, comprising: means for providing differential correction signals in a **first standard format** for various ones of a plurality of satellites, wherein the differential correction signals include range error correction signals and range rate error correction information; means for converting said differential correction signals in the **first standard format** to signals in a **second standard format;** means for prioritizing the broadcast transmission time of the signals in the **second standard format** , wherein the means for prioritizing the transmission time of the signals in the **second standard format** includes means for prioritizing according to the range error corrections signals for the various satellites; transmitter means for broadcasting a signal modulated by the prioritized signals in the **second standard format;** receiver means for receiving and demodulating the broadcast signal modulated by the prioritized signals in the **second standard format;** means for reconverting the broadcast prioritized signals in the **second standard format** to provide differential correction signals in the **first standard format.**

28. A system for broadcasting differential correction signals for a global positioning system (GPS) which includes a plurality of orbiting satellites, comprising: means for providing differential correction signals in a **first standard format** for various ones of a plurality of satellites; means for converting said

differential correction signals in the **first standard format** to signals in a **second standard format**, wherein the **second standard format** is a Radio Data Service (RDS) standard format; means for prioritizing the broadcast transmission time of the signals in the **second standard format**; transmitter means for broadcasting a signal modulated by the prioritized signals in the **second standard format**; receiver means for receiving and demodulating the broadcast signal modulated by the prioritized signals in the **second standard format**; means for reconverting the broadcast prioritized signals in the **second standard format** to provide differential correction signals in the **first standard format**.

29. A system for broadcast transmitting differential correction signals for a global positioning system GPS which includes a plurality of orbiting satellites, comprising: means for providing differential correction signals in a **first standard format** for various ones of a plurality of satellites; means for converting said differential correction signals in the **first standard format** to provide signals in a **second standard format**, wherein the differential correction signals include range error correction signals and range rate error correction information; means for prioritizing the broadcast transmission time of the signals in the **second standard format**, wherein the means for prioritizing the broadcast transmission time of the signals in the **second standard format** includes means for prioritizing according to the maximum range acceleration rate for the various satellites; transmitter means for broadcasting a signal modulated by the prioritized signals in the **second standard format**.

30. A system for broadcast transmitting differential correction signals for a global positioning system GPS which includes a plurality of orbiting satellites, comprising: means for providing differential correction signals in a **first standard format** for various ones of a plurality of satellites; means for converting said differential correction signals in the **first standard format** to provide signals in a **second standard format**, wherein the differential correction signals include range error correction signals and range rate error correction information; means for prioritizing the transmission time of the signals in the **second standard format**, wherein the means for prioritizing the transmission time of the signals in the **second standard format** includes means for prioritizing according to the range acceleration rate for the various satellites exceeding a predetermined absolute value; transmitter means for broadcasting a signal modulated by the prioritized signals in the **second standard format**.

31. A system for broadcast transmitting differential correction signals for a global positioning system GPS which includes a plurality of orbiting satellites, comprising: means for providing differential correction signals in a **first standard format** for various ones of a plurality of satellites; means for converting said differential correction signals in the **first standard format** to provide signals in a **second standard format**, wherein the differential correction

signals include range error correction signals and range rate error correction information; means for prioritizing the transmission time of the signals in the **second standard format,**
wherein the means for prioritizing the transmission time of the signals in the **second standard format** includes
means for prioritizing according to range error correction signals exceeding a predetermined absolute value; transmitter means for broadcasting a signal modulated by the prioritized signals in the **second standard format.**

32. A system for broadcast transmitting differential correction signals for a global positioning system GPS which includes a plurality of orbiting satellites, comprising: means for providing differential correction signals in a **first standard format** for various ones of a plurality of satellites; means for converting said differential correction signals in the **first standard format** to provide signals in a **second standard format,** wherein the differential correction signals include range error correction signals and range rate error correction information; means for prioritizing the transmission time of the signals in the **second standard format,**
wherein the means for prioritizing the transmission time of the signals in the **second standard format** includes
means for prioritizing according to the range error corrections signals for the various satellites; transmitter means for broadcasting a signal modulated by the prioritized signals in the **second standard format.**

33. A system for broadcast transmitting differential correction signals for a global positioning system GPS which includes a plurality of orbiting satellites, comprising: means for providing differential correction signals in a **first standard format** for various ones of a plurality of satellites; means for converting said differential correction signals in the **first standard format** to provide signals in a **second standard format,** wherein the **second standard format** is a Radio Data Service (RDS) standard format; means for prioritizing the transmission time of the signals in the **second standard format;** transmitter means for broadcasting a signal modulated by the prioritized signals in the **second standard format.**

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L6 ANSWER 1 OF 2 USPATFULL
PI US 6078350 , 20000620
SUMM According to one embodiment, the present invention is directed to a method and arrangement for video conferencing. One aspect of the invention is directed to a system for transmitting encoded video data between a first video conferencing terminal and a second video conferencing terminal, the first video conferencing terminal compatible with a **first format** of encoded video data, and the second video conferencing terminal compatible with a **second format** of encoded video data, comprising: a first node **configured** and arranged to couple to the first video conferencing terminal and including a first decoder **configured** and arranged to receive encoded video data of the **first format** from the **first** video conferencing terminal and **decode** the **video data**; and a first encoder coupled to the first decoder and **configured** and arranged to receive **decoded video data** from the **decoder** and encode the **decoded video data** in the **second format**; the arrangement further comprising a second node **configured** and arranged to couple to the second video conferencing terminal and including a second decoder **configured** and arranged to receive encoded video data of the **second format** from the **second** video conferencing terminal and **decode** the **video data**; and a second encoder coupled to the second decoder and **configured** and arranged to receive **decoded video data** from the **decoder** and encode the **decoded video data** in the **first format**; and the arrangement lastly comprising a switch circuit arrangement coupled to the first node and coupled to the second node, wherein the first node is arranged to provide encoded video data of the **first format** from the **second** node to the first video conferencing terminal, and the second node is arranged to provide encoded video data of the **second format** from the **first** node to the second video conferencing terminal.

DETD FIGS. 3A, 3B, and 3C contain a flowchart of an example method operating in accordance with the present invention. At processing block 302, an example switch receives a request to establish a video conference session between a first video conference terminal and a second video conference terminal. The switch then determines the expected format of encoded video data for each of the first and second video conferencing terminals, as shown by processing block 304. Processing continues at block 306 where the switch **configures** a first node to the **decode video data** of the **first format** from the **first** video conferencing terminal and encode the video data into the **second format**. Continuing with processing block 308, the switch also **configures** a second node to **decode video data** of the **second format** from the **second** terminal and encode the video data into the **first format**. Thus, after processing block 308, two translator nodes are established, one for translating from format A to format B and a second for translating from format B to format A.

CLM What is claimed is:
1. A system for transmitting encoded video data between a first video conferencing terminal and a second video conferencing terminal, the first video conferencing terminal compatible with a **first format** of encoded video data, and the second video conferencing terminal compatible with a **second format** of encoded

video data, comprising: a first node **configured** and arranged to couple to the first video conferencing terminal and including a first decoder **configured** and arranged to receive encoded video data of the **first format** from the **first** video conferencing terminal and **decode** the **video data**; and a first encoder coupled to the first decoder and **configured** and arranged to receive **decoded video data** from the **decoder** and encode the **decoded video data** in the **second format**; a second node **configured** and arranged to couple to the second video conferencing terminal and including a second decoder **configured** and arranged to receive encoded video data of the **second format** from the **second** video conferencing terminal and **decode** the **video data**; and a second encoder coupled to the second decoder and **configured** and arranged to receive **decoded video data** from the **decoder** and encode the **decoded video data** in the **first format**; and a switch circuit arrangement coupled to the first and second nodes by communications lines provided by a public switch telephone line provider, wherein the first node is arranged to provide encoded video data of the **first format** from the **second** node to the first video conferencing terminal, and the second node is arranged to provide encoded video data of the **second format** from the **first** node to the second video conferencing terminal.

10. A system for transmitting encoded video data between a first video conferencing terminal and a second video conferencing terminal, the first video conferencing terminal compatible with a **first format** of encoded video data, and the second video conferencing terminal compatible with a **second format** of encoded video data, comprising: a first node **configured** and arranged to couple to the first video conferencing terminal and including a first decoder **configured** and arranged to receive encoded video data of the **first format** from the **first** video conferencing terminal and **decode** the **video data**; and a first encoder coupled to the first decoder and **configured** and arranged to receive **decoded video data** from the **decoder** and encode the **decoded video data** in the **second format**; a second node **configured** and arranged to couple to the second video conferencing terminal and including a second decoder **configured** and arranged to receive encoded video data of the **second format** from the **second** video conferencing terminal and **decode** the **video data**; and a second encoder coupled to the second decoder and **configured** and arranged to receive **decoded video data** from the **decoder** and encode the **decoded video data** in the **first format**; and a switch circuit arrangement coupled to the first node and coupled to the second node, wherein the first node is arranged to provide encoded video data of the **first format** from the **second** node to the first video conferencing terminal, and the second node is arranged to provide encoded video data of the **second format** from the **first** node to the second video conferencing terminal; and wherein the first video conferencing terminal and the first node are co-located at a first station, the second video conferencing terminal and the second node are co-located at a second station, and wherein the first and second

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L4 ANSWER 2 OF 4 USPATFULL
PI US 5982432 19991109
SUMM In the above configuration, a plurality of digital picture signals **compressed** in a **first format** is **decoded** to a plurality of non-compressed picture signals of a 4:1:1 color component type, the non-compressed picture signals of the 4:1:1 color component type are directly converted into a plurality of converted color difference signals of a 4:2:0 color component type. In this conversion, color difference signals are removed on every other row from the color difference signals of the 4:1:1 color component type and color difference signals are added on every other column to remaining color difference signals. Therefore, a plurality of converted color difference signals of the 4:2:0 color component type, in which the number of signals in the y direction is half that of color difference signals of the 4:1:1 color component type and the number of converted color difference signals in the x direction is double that of color difference signals of the 4:1:1 color component type, are produced. Values of the converted color difference signals are determined according to values of the color difference signals of the 4:1:1 color component type. Thereafter, luminance signals of the non-compressed picture signals and the converted color difference signals of the 4:2:0 color component type are combined to produce non-compressed picture signals of the 4:2:0 color component type. Thereafter, the non-compressed picture signals of the 4:2:0 color component type are coded to a plurality of digital picture signals compressed in a **second format**.

SUMM In the above configuration, a plurality of digital picture signal **compressed** in a **first format** are **decoded** to a plurality of DCT coefficients of non-compressed picture signals of a 4:1:1 color component type, the DCT coefficients are converted into a plurality of DCT coefficients of non-compressed picture signals of a 4:2:0 color component type, a plurality of non-compressed picture signals of the 4:2:0 color component type are produced from the DCT coefficients of the non-compressed picture signals of the 4:2:0 color component type, and the non-compressed picture signals of the 4:2:0 color component type are coded to a plurality of digital picture signals compressed in a **second format** .

CLM What is claimed is:
36. A picture providing system, comprising: picture input means for receiving a plurality of digital picture signals compressed in a first format; picture reproducing means for reproducing a digital picture according to a plurality of digital picture signals compressed in a **second format** different from the first format; picture providing means for receiving the digital picture signals compressed in the first format from the picture input means, converting the digital picture signals compressed in the first format into the digital picture signals compressed in the **second format** and transmitting the digital picture signals compressed in the **second format** to the picture reproducing means; and a network through which the digital picture signals compressed in the first format is transmitted from the picture input means to the picture providing means and the digital picture signals compressed in the **second format** is transmitted from the picture providing means to the picture reproducing means, the picture providing means comprising: communicating means for receiving the digital picture signals compressed in the first format from the picture input means

through the network and outputting the digital picture signals compressed in the **second format** to the picture reproducing means through the network; and picture signal converting means for converting the digital picture signals of the first format received by the communicating means into the digital picture signals compressed in the **second format** and outputting the digital picture signals compressed in the **second format** to the communicating means, and the picture signal converting means comprising picture **decoding** means for **decoding** the digital picture signals **compressed** in the **first format** to produce a plurality of non-compressed picture signals of a 4:1:1 color component type, the non-compressed picture signals being arranged in a matrix of rows and columns; component signal converting means for directly converting color difference signals of the non-compressed picture signals obtained by the picture decoding means into converted color difference signals of a 4:2:0 color component type by removing color difference signals on every other row from the color difference signals of the non-compressed picture signals to halve the number of color difference signals in a y direction and adding a color difference signal to a position between each pair of color difference signals adjacent to each other in an x direction to double the number of color difference signals in the x direction, setting values of the converted color difference signals of the 4:2:0 color component type according to values of the color difference signals of the non-compressed picture signals obtained by the picture decoding means and combining luminance signals of the non-compressed picture signals obtained by the picture decoding means and the converted color difference signals of the 4:2:0 color component type obtained by the color difference signal converting means for each pixel of the frame to produce non-compressed picture signals of the 4:2:0 color component type; and picture coding means for coding the non-compressed picture signals of the 4:2:0 color component type obtained by the component signal converting means to produce the digital picture signals compressed in the **second format**.

L4 ANSWER 3 OF 4 USPATFULL
PI US 5832085 19981103
CLM What is claimed is:
6. A system for recording in a predefined compressed format an input data stream composed of packets comprising: a packet decode for determining whether the input data packet is in the predefined compressed format; a first decoder that extracts audio/video data from the packet and selectively forwards header and audio/video information to a switch and normal play video data to a multiplexer if the input data stream is in the predefined **compressed format**, said **first decoder** further issuing a first audio control signal to the switch if the audio/video information comprises audio data; a second decoder that extracts audio/video data from the input data packet and selectively forwards audio/video information and header information to the switch and normal play video data to the multiplexor if the input data stream is in an alternate **format**, said **second** decoder further issuing a second audio control signal to the switch if the audio/video information comprises audio data; said switch selectively forwarding the audio/video information to audio recording circuitry to generate audio normal play data based on the first audio control signal and the second audio control signal, said switch alternately forwarding the header and audio/video information to a packetizer; said packetizer generating header data that is compatible with the predefined compressed format, said packetizer further

stations are communicatively coupled to one another via a communications line.

12. A system for transmitting encoded video data between a first video conferencing terminal and a second video conferencing terminal, the first video conferencing terminal compatible with a **first format** of encoded video data, and the second video conferencing terminal compatible with a **second format** of encoded video data, comprising: a first node **configured** and arranged to couple to the first video conferencing terminal and including a first decoder **configured** and arranged to receive encoded video data of the **first format** from the **first** video conferencing terminal and **decode** the **video data**; and a first encoder coupled to the first decoder and **configured** and arranged to receive **decoded video data** from the **decoder** and encode the **decoded video data** in the **second format**; a second node **configured** and arranged to couple to the second video conferencing terminal and including a second decoder **configured** and arranged to receive encoded video data of the **second format** from the **second** video conferencing terminal and **decode** the **video data**; and a second encoder coupled to the second decoder and **configured** and arranged to receive **decoded video data** from the **decoder** and encode the **decoded video data** in the **first format**; and a switch circuit arrangement coupled to the first and second by a POTS communications channel, wherein the first node is arranged to provide encoded video data of the **first format** from the **second** node to the first video conferencing terminal, and the second node is arranged to provide encoded video data of the **second format** from the **first** node to the second video conferencing terminal.

L6 ANSWER 2 OF 2 USPATFULL
PI US 5654751 19970805
CLM What is claimed is:

9. A testing jig for testing the compressed digital input into and output from a settop box in a digital network transporting source video, said settop box containing a network interface module for receiving and converting data derived from a first compressed digital video data signal having a **first format** into a **second** video data signal having a **second format** and for forwarding said second **video data** signal to a **decoder** engine **decoding** said second **video data** signal over a NIM interface, said testing jig comprising: a memory for storing a test sequence of video data of said **second format**; an output interface for forwarding the video data of said **second format** to said decoder engine over said interface module; and a processing circuit for controlling the outputting of said stored test sequence of video data of said **first format** to the output interface as video data of said **second format**, wherein said testing jig is **configured** to be of the same physical **configuration** as said network interface module and wherein said testing jig tests digital video input into or output from said decoder engine by replacing said network interface module.

14. A method for testing in a digital network transporting source video

generating dummy data to be included in an output packet if the input data packet is shorter in length than the output packet; and said multiplexor coupled to receive header data, dummy data, video normal play data and audio normal play data as input, said inputs multiplexed as output to form the output packet.

L4 ANSWER 4 OF 4 USPATFULL
PI US 5757967 19980526
CLM What is claimed is:

15. A video decoder and format converter, comprising: a shared common memory; a decoder having an input for receiving a compressed video stream and an output for providing to the common memory, pictures of a **first format decoded** from the **compressed** video stream; and, a format converter having an input connected to receive the pictures from the shared common memory and an output for providing reformatted picture of a **second** display **format** formed from information extracted from a plurality of the pictures in the shared common memory.

19. An apparatus for changing the format and frame rate of interframe encoded video, comprising: a shared common memory; a decoder having an input for receiving a compressed video stream and an output for providing to the common memory, pictures of a **first format decoded** from the **compressed** video stream; and, a format and frame rate converter having an input connected to receive the pictures from the shared common memory and an output for providing reformatted picture of a **second** display **format** and a **second** display rate formed from information extracted from a plurality of the pictures in the common memory; decoder controller means, coupled to said decoder, for determining when storage of reconstructed pictures in the common memory will interfere with the extraction and pausing the decoder in response to a determination that the storage will interfere; and, a memory management system, coupled to said common memory, said memory management system including means for identifying picture information that is likely to be needed to decode a future picture and means for directing memory writes to memory locations in said shared common memory not currently storing information is likely to be needed to decode a future picture.

21. An apparatus capable of displaying video images, comprising: a display device; a source of compressed video; a video decoder and format converter, having: a shared common memory; a decoder having an input for receiving the compressed video from the source and an output for providing to the shared common memory, pictures of a **first format decoded** from the **compressed** video; and, a format converter having an input connected to receive the pictures from the common memory and an output for providing to the display device, reformatted pictures of a **second** display **format**, each of the reformatted pictures being formed from information extracted from a plurality of the pictures in the shared common memory.

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through an encoder encoding said source video into a first encoded video data signal using a **first format** to at least one
settop box containing a network interface module (NIM) for receiving and converting data derived from said first encoded video data signal into a second video data signal through a NIM interface and for forwarding said second **video data** signal to a **decoder**
engine **decoding** said second **video data**
signal, said method comprising the steps of: replacing said network interface module of said settop box with a testing jig, said testing jig being of the same physical **configuration** as said network
interface module; encoding test video into encoded test video data of said **first format**; inputting said encoded test video
data of said **first format** into an input interface of
said testing jig; converting said encoded test video data of said **first format** into test video data of said
second format in said testing jig; and forwarding said
test video data of said **second format** from said
testing jig to said decoder engine over said NIM interface.

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L12 ANSWER 2 OF 12 USPATFULL
PI US 6256354 B1 20010703
SUMM One embodiment of the present invention is a circuit comprising a first receiving channel circuit coupled to receive a first incoming voice signal received by the portable station from a wireless interface. Furthermore, the first receiving channel circuit is for **decoding** the first incoming voice signal from a **first** data **format** to a **second** data **format**. The circuit further comprises a first transmitting channel circuit communicatively coupled to the first receiving channel circuit to receive the first incoming voice signal in the **second** data **format** and for encoding the first incoming voice signal from the **second** data **format** to a third data format. The circuit also comprises a memory device coupled to the transmitting channel circuit to receive the first incoming voice signal in the third data format and for storing the first incoming voice signal in the third data format. The third **data** format is a **compression** of the **first** **data format**.

CLM What is claimed is:
1. A circuit for encoding and **decoding** voice signals within a portable station of a personal handy phone system, said circuit comprising: a first receiving channel circuit coupled to receive a first voice signal over a wireless interface and for **decoding** said first voice signal from a **first** data **format** to a **second** data **format**; a converter circuit coupled to receive said first voice signal in said **second** data **format** and for converting said first voice signal from said **second** data **format** to an analog data format, said converter circuit also coupled to receive a second voice signal in said analog data format and for converting said second voice signal from said analog data **format** to said **second** data **format**; a first buffer device for storing said first voice signal in said **second** data **format**; a second buffer device for storing said second voice signal in said **second** data **format**; a controller circuit coupled to said first and second buffer devices and for mixing said first and second voice signals to produce a conversation signal in said **second** data **format**; a third buffer device for storing said conversation signal; a first transmitting channel circuit coupled to said third buffer device to receive said conversation signal and for encoding said conversation signal from said **second** data **format** to a third data format, said third **data** format being a **compression** of said **first data** **format**; and a memory device coupled to said first transmitting channel circuit to receive said conversation signal and for storing said conversation signal in said third data format.

10. An apparatus for encoding and **decoding** voice signals within a portable station of a personal handy phone system, said apparatus comprising: a first receiving channel means coupled to receive a first voice signal over a wireless interface and for **decoding** said first voice signal from a **first** data **format** to a **second** data **format**; a converter means coupled to receive said first voice signal in said **second** data **format** and for converting said first voice signal from said **second** data **format** to an analog data format, said converter means also coupled to receive a second voice signal in said analog data format and for converting said second voice signal from said

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analog data **format** to said **second** data **format**; a first buffer means for storing said first voice signal in said **second** data **format**; a second buffer means for storing said second voice signal in said **second** data **format**; a controller means coupled to said first and second buffer means and for mixing said first and second voice signals to produce a conversation signal in said **second** data **format**; a third buffer means for storing said conversation signal; a first transmitting channel means coupled to said third buffer means to receive said conversation signal and for encoding said conversation signal from said **second** data **format** to a third data format, said third **data** format being a **compression** of said **first data format**; and a memory means coupled to said first transmitting channel means to receive said conversation signal and for storing said conversation signal in said third data format.

L12 ANSWER 3 OF 12 USPATFULL
PI US 6249617 B1 20010619
CLM What is claimed is:
6. In a system having a memory for storing data in a **first** predetermined **format**, a video compressor coupled to the memory comprising: a. a **compression** engine for **compressing data**, the **compression** engine accepting **data** in a **second** predetermined **format** different from the **first** predetermined **format**; b. an address generator for generating addresses to access the memory for data in the **first** predetermined **format**; and c. an integrated scaling mechanism for scaling the data in the **first** predetermined **format** into data in the **second** predetermined **format** acceptable to the compression engine, said scaling mechanism having an input for receiving data in a **first** predetermined **format** and an output coupled to the **compression** engine for providing **data** in the **second** predetermined **format**, wherein the integrated scaling mechanism further includes: a buffer having a plurality of storage locations arranged in row and columns; a row-**decoder** for receiving a portion of an address and based thereon for selecting a row; a column-**decoder** for receiving a portion of the address and based thereon for selecting a column; and a multiplexer interposed between the row **decoder** and each row for selectively performing either one of (i) enabling a current row or (ii) simultaneously enabling a current row and a next row based on an up-insert signal.

Mackly Monestime

L2 ANSWER 5 OF 24 USPATFULL
PI US 6259891 B1 20010710
CLM What is claimed is:

8. The adapter of claim 7, further comprising fourth means for receiving a control signal from the satellite integrated receiver/**decoder** in a **first format**, further means for converting the control signal to a **second format**, and means for delivering the control signal in the **second format** to the processor.

14. A direct broadcast satellite (DBS) video communication system adapted to be coupled to a display device the communication system comprising: a satellite integrated receiver/decoder; a wireless local area network transceiver; and an adapter coupled between the satellite integrated receiver/decoder and the wireless local area network transceiver, said adapter including: first means for receiving a first video signal from the satellite integrated receiver/decoder; second means for receiving a data signal from the wireless local area network transceiver; means for combining the data signal with the first video signal to produce a second video signal; means for transmitting the second video signal to the display device; further means for receiving an information signal from the satellite integrated receiver/**decoder** in a **first format** suitable for transmission by a telephone network; means for converting the information signal to a **second format** suitable for transmission by a wireless local area network; and means for delivering the information signal in the **second format** to the wireless local area network transceiver.

```
L1          172 S DRAM (5A) (MULTIPLE OR PLURALITY OR MORE THAN ONE) (3W)
STORA
L2         7952 S STOR? (3A) DIGITAL DATA
L3          367 S MEDIA PROCES?
L4         3634 S MEDIA (2A) PROCES?
L5            0 S L1 (P) L4
L6            9 S L2 (P) L4
L7          139 S DIGITAL DATA (4A) VIDEO (3A) COMPRES?
L8           96 S STANDARD? (3A) COMPRES? (2A) VIDEO DATA
L9           20 S STANDARD? (3A) COMPRES? VIDEO DATA
L10           0 S L9 (P) L1
L11           0 S L7 (P) L1
L12           0 S L7 AND L1
L13           1 S L9 (P) DECOD?
L14          22 S L7 (P) DECOD?
L15           0 S L14 (P) DRAM
L16           3 S L14 AND DRAM
```

L1	934	S	(345/541 OR 345/555 OR 345/155 OR 345/431)/NCL
L2	249	S	L1 AND (STOR? OR ADDRES?) (2A) LOCATION#
L3	6	S	L1 AND SINGLE CLOCK CYCLE
L4	23	S	L1 AND ONE CLOCK CYCLE
L5	25	S	L3 OR L4
L6	9	S	L5 AND COMPRES? (3A) DATA
L7	9	S	L6 AND PROCES?
L8	3	S	L6 AND DRAM

read out from said pair of DRAMs is continuously supplied to said game decoder elements.

L16 ANSWER 2 OF 3 USPATFULL

SUMM According to another aspect of the present invention, an apparatus comprises an MPEG **decoder**. This **decoder** decompresses a first stream of **compressed, digital data** into first **video** data having a first resolution. The **decoder** also partially decompresses a second stream of **compressed, digital data** into second **video** data having a second resolution less than the first resolution. The first and second video data represent first and second video programs, respectively. An overlay controller receives the first and second video data, and in response outputs a video frame signal simultaneously displaying at least portions of the first and second video programs. Hence, the apparatus uses a single MPEG **decoder** to obtain first and second video data representing first and second video programs, respectively, and an overlay controller to simultaneously display at least portions of the first and second video programs. The MPEG **decoder** performs the partial decompression of the second stream during idle intervals between frames from the first stream of compressed, digital data.

DETD According to the embodiment of FIG. 5, the MPEG video decoder is an application specific IC (ASIC) dedicated to decode only one video program. Hence, the second (PIP) video program is decoded by the interactive application software 102. The interactive application processor 102 comprises a general purpose microprocessor or RISC device such as the commercially-available Motorola Power PC, and any required memory such as application **DRAM**, non-volatile RAM, ROM, EEPROM, and flash memory. The processor 102 executes software having a routine for partially decompressing MPEG-encoded data and outputting decompressed video data at a reduced frame rate, for example 10 frames per second. Specifically, the processor 102 executes software to parse the transport packets of the secondary (PIP) program and remove the video elementary stream data. The video elementary stream data will then be decoded by the interactive application processor 102.

CLM What is claimed is:

11. An apparatus comprising: a digital video processor decompressing a first stream of **compressed, digital data** representing a first **video** program into decompressed first video data having a first resolution, the digital video Processor outputting a video signal representing a frame of said first video data having a portion overlaid by decompressed second video data having a corresponding second resolution less than the first resolution; and an application processor partially decompressing a second stream of **compressed, digital data** representing a second **video** program into said second video data; wherein: the first and second streams carry MPEG-encoded video data having respective identifiers; the application processor comprises a microprocessor and a MPEG demultiplexer selectively routing the first and second streams to the digital video processor and the microprocessor in response to the respective identifiers; and the digital video processor comprises: (1) an MPEG **decoder** decompressing the MPEG-encoded video data from the first stream, and (2) a graphics overlay controller receiving the first and second video data at first and second frame rates, respectively, and in response generating said video signal.

25. The apparatus of claim 24, wherein the digital video processor comprises: a digital **video decoder** decompressing the

compressed, digital data from the first stream into s[redacted] first video data; and a video [redacted]erlay controller combining the first and second decompressed video data into said video signal.

42. An apparatus comprising: an MPEG **decoder** decompressing a first stream of **compressed, digital data** into first decompressed **video** data having a first resolution and partially decompressing a second stream of **compressed, digital data** into second decompressed **video** data having a second resolution less than the first resolution, the first and second decompressed video data representing first and second video programs, respectively; and an overlay controller receiving the first and second decompressed video data and in response outputting a video frame signal simultaneously displaying at least portions of the first and second video programs.

L16 ANSWER 3 OF 3 USPATFULL

DETD File librarian 250 controls distribution of video, audio, still image data and text selections to session manager 290 in response to information requests from session manager 290 and video file application processor 370. Referring to FIG. 15, the Librarian further monitors and record in feature index 252 the storage location of all video selections for video-on-demand and video file applications. The librarian 250 also records a history of access to video programming, i.e., "features" and to other data provided during each twenty-four hour period in usage data accumulation system 260. The usage data is supplied to usage probability processor 262 to establish an intelligent cache using **DRAM** Storage 278 for rapid access and highly addressable storage of features.

DETD Usage probability processor 262 statistically determines features having the highest probability of usage on a per hour, day of week basis to properly allocate high order storage, i.e., **DRAM** storage 278, on an hourly basis. In support of this function, usage data accumulation 260 stores tables of data including time of viewing, day of viewing and cumulative number of requests each time a feature is supplied.

DETD Allocation of storage in the file server 242, 244 is based on the ranking of a feature and the output of the trend processing performed by usage probability processor 262. Storage is divided into several components, including **DRAM** 278, magnetic disk 282, high speed magnetic tape 286 and archival magnetic tape 290. All features are stored on the appropriate media based on the priority ranking of the feature. For example, **DRAM** storage 278 is used for the highest priority features as determined by the trend processing whereas archival storage is used for the lowest priority features. Table 2 gives typical priority assignments and storage capabilities of each media.

DETD TABLE 2

Priority	Number of Features	Storage
1	20 .+-. 5	**DRAM**
2	100 .+-. 20	MAGNETIC DISK
3	300 .+-. 50	HIGH SPEED TAPE
4	500 +	ARCHIVAL TAPE

DETD **DRAM** storage 278 in the described embodiment is used for the highest twenty features and data files as determined by the trend processing. When a feature or other high priority media file is stored in **DRAM**, it does not occupy magnetic storage space until removed from **DRAM** storage. A compressed feature length movie of 90 minutes duration occupies approximately 1.2 gigabytes.

DETD Disk storage units 282 are fast access magnetic and/or optical media providing storage for the second highest fifty priority features and media data files as determined by the trend processing. When a feature is stored on a Disk unit, it does not occupy **DRAM** or tape storage until removed.

CLM What is claimed is:

12. The network of claim 11, wherein said digital **video** signals comprise **compressed digital data** signals, and said **decoder** includes a decompressor for decompressing an incoming video digital data signal and producing analog video and associated audio output signals.

L16 ANSWER 1 OF 3 USPATFULL
PI US 6212681 20010403
WO 9721308 19970612

L16 ANSWER 2 OF 3 USPATFULL
PI US 5847771 19981208

L16 ANSWER 3 OF 3 USPATFULL
PI US 5410343 19950425

L18 ANSWER 1 OF 1 USPATFULL

AB Two MPEG-encoded digital data streams are simultaneously decoded in a digital entertainment terminal to provide Picture-in-Picture (PIP) and Picture-on-Picture (POP) capabilities for a conventional television. A primary MPEG-encoded data stream is decoded using a digital video processor optimized for MPEG2 decoding or a dedicated MPEG2 decoder system. A secondary MPEG-encoded data stream is partially processed by filtering the B frames of the secondary MPEG-encoded data stream and using the corresponding I and P frames in a partial decoding arrangement to obtain decompressed video data providing a limited-resolution representation of a second program. Partial decoding may also be performed using only I frames. The partial decoding may be implemented through execution of software by a general-purpose microprocessor. Alternatively, the **media processor** may perform the partial decoding during the idle intervals of the dedicated **media processor**.

SUMM According to another aspect of the present invention, an apparatus comprises an MPEG **decoder**. This **decoder** decompresses a first stream of **compressed, digital data** into first **video** data having a first resolution. The **decoder** also partially decompresses a second stream of **compressed, digital data** into second **video** data having a second resolution less than the first resolution. The first and second video data represent first and second video programs, respectively. An overlay controller receives the first and second video data, and in response outputs a video frame signal simultaneously displaying at least portions of the first and second video programs. Hence, the apparatus uses a single MPEG **decoder** to obtain first and second video data representing first and second video programs, respectively, and an overlay controller to simultaneously display at least portions of the first and second video programs. The MPEG **decoder** performs the partial decompression of the second stream during idle intervals between frames from the first stream of compressed, digital data.

DETD FIGS. 3 and 5 are block diagrams illustrating different embodiments of the DET 52 of the present invention. The DET 52 portion of the set-top device in FIG. 3 includes an application processor 74, a digital video processor 75, and a peripheral interface 78. The DET 52 also includes non-volatile random access memory 80a, 80b for example electrically erasable programmable read only memory (EEPROM) or flash memory. Specifically, the DET 52 includes a RAM 80a for use by the application processor 74, and the digital video processor 75 comprises a **media processor** 76 and a RAM 80b. The RAM 80a and 80b each have a non-volatile portion for storing the operating system and software programming for the application processor 74 and the **media processor** 76, respectively. The software stored in the RAM 80a and 80b defines the basic functionality of the respective processors 74 and 76 in the DET 52. For example, the operating system stored in the RAM 80a controls how the application processor 74 interprets application programs. The operating system stored in the RAM 80a also includes the various driver routines permitting the application

processor to operate the other elements of the DET. The operating system
stored in the RAM 80a and 80b also includes the basic or `resident` application under which the DET operates when not running a downloaded application. The resident application preferably emulates a cable television type program reception type user interface for the particular
network to which the set-top connects.

DETD According to the embodiment of FIG. 3, the DET 52 operates as a distributed processing system, where the application processor 74 performs the background DET functions including control of DET operations, execution of downloaded applications, user interface functions, and generating upstream channel request and signaling messages in response to user inputs. The digital video processor 75 is a
processing system dedicated to decompressing and decoding MPEG encoded data. The **media processor** 76 of FIG. 3 may be
implemented as an enhanced microprocessor having multimedia-specific and
digital signal processing instruction sets. The **media processor** 76 also includes high-bandwidth I/O to perform
multimedia operations and MPEG decoding in real time. Hence, the RAM 80b
stores operating system programming and instruction sets for optimized MPEG2 decoding and multimedia applications.

DETD As described above, the software controlling operation of the **media processor** in partially decompressing the
secondary (PIP) transport stream is stored as a modified instruction set
in the RAM 80b. The software may be downloaded by a technician via the interface 78 which can accommodate, for example, a PCMCIA card. Preferably, however, the software is downloaded from the network 10, for
example as an enhanced service offered by the VIP 12. Specific details about downloading software into the DET 52 is disclosed in the above-incorporated application Ser. No. 08/498,265 (attorney docket 680-083D).

DETD Another variation of the disclosed embodiments involves fully decoding only a viewed portion of the primary program. Specifically, overlaying the secondary (PIP) program over the primary program causes a portion of
the primary program of interest to be covered up by the PIP inset. Since
the covered portion of the primary image is not visible to the viewer, it does not need to be fully decoded. Hence the **media processor** of FIG. 3 and the MPEG2 decoder 104 of FIG. 5 can be
freed from the responsibility of fully decoding the covered portion of the primary video, so that significant processing power may be freed up for other tasks, such as decoding the PIP image.

CLM What is claimed is:

11. An apparatus comprising: a digital video processor decompressing a first stream of **compressed, digital data**
representing a first **video** program into decompressed first video data having a first resolution, the digital video Processor outputting a video signal representing a frame of said first video data having a portion overlaid by decompressed second video data having a corresponding second resolution less than the first resolution; and an application processor partially decompressing a second stream of **compressed, digital data** representing a
second **video** program into said second video data; wherein: the first and second streams carry MPEG-encoded video data having respective
identifiers; the application processor comprises a microprocessor and a MPEG demultiplexer selectively routing the first and second streams to

the digital video processor and the microprocessor in response to the respective identifiers; and the digital video processor comprises: (1) an MPEG **decoder** decompressing the MPEG-encoded video data from the first stream, and (2) a graphics overlay controller receiving the first and second video data at first and second frame rates, respectively, and in response generating said video signal.

12. An apparatus comprising: a digital video processor decompressing a first stream of compressed, digital data representing a first video program into decompressed first video data having a first resolution, the digital video processor outputting a video signal representing a frame of said first video data having a portion overlaid by decompressed second video data having a corresponding second resolution less than the first resolution; and an application processor partially decompressing a second stream of compressed, digital data representing a second video program into said second video data; wherein the digital video processor comprises: a **media processor** decompressing said first stream of compressed, digital data; and a memory storing code executable by the **media processor** to control the decompressing of the first stream of compressed, digital data.

25. The apparatus of claim 24, wherein the digital video processor comprises: a digital **video decoder** decompressing the **compressed, digital data** from the first stream into said first video data; and a video overlay controller combining the first and second decompressed video data into said video signal.

28. The apparatus of claim 24, wherein the digital video processor comprises: a **media processor** decompressing the first stream of compressed, digital data; and a memory storing code executable by the **media processor** to control the decompressing of the first stream of compressed, digital data.

29. A digital entertainment terminal comprising: an application processor receiving multiplexed digital data carrying first and second streams of compressed, digital data representing first and second programs, respectively, the first and second streams having first and second identifiers, respectively, the application processor outputting the first stream of compressed digital data and a portion of the second stream of compressed, digital data in response to the respective first and second identifiers; and a **media processor** decompressing at least the first stream into first decompressed video data representing said first program, the **media processor** combining said first decompressed video data with second decompressed video data generated from said portion of the second stream and outputting the combined first and second video data as a video signal representing a video frame simultaneously displaying at least portions of said first and second video programs; wherein said portion of the second stream is partially decompressed into said second decompressed video data by one of said application **processor** and said **media processor**.

30. The terminal of claim 29, further comprising a buffer memory receiving from the application processor and storing the first stream and said portion of the second stream received from the **media processor**.

38. The terminal of claim 29, wherein the **media processor** partially decompresses a frame from said portion of the second stream between the decompression of two adjacent frames from said first stream.

42. An apparatus comprising: an MPEG **decoder** decompressing a first stream of **compressed, digital data** into first decompressed **video** data having a first resolution and partially decompressing a second stream of **compressed, digital data** into second decompressed **video** data having a second resolution less than the first resolution, the first and second decompressed video data representing first and second video programs, respectively; and an overlay controller receiving the first and second decompressed video data and in response outputting a video frame signal simultaneously displaying at least portions of the first and second video programs.

L18 ANSWER 1 OF 1 USPATFULL

AB Two MPEG-encoded digital data streams are simultaneously decoded in a digital entertainment terminal to provide Picture-in-Picture (PIP) and Picture-on-Picture (POP) capabilities for a conventional television. A primary MPEG-encoded data stream is decoded using a digital video processor optimized for MPEG2 decoding or a dedicated MPEG2 decoder system. A secondary MPEG-encoded data stream is partially processed by filtering the B frames of the secondary MPEG-encoded data stream and using the corresponding I and P frames in a partial decoding arrangement to obtain decompressed video data providing a limited-resolution representation of a second program. Partial decoding may also be performed using only I frames. The partial decoding may be implemented through execution of software by a general-purpose microprocessor. Alternatively, the **media processor** may perform the partial decoding during the idle intervals of the dedicated **media processor**.

SUMM According to another aspect of the present invention, an apparatus comprises an MPEG **decoder**. This **decoder** decompresses a first stream of **compressed, digital data** into first **video** data having a first resolution. The **decoder** also partially decompresses a second stream of **compressed, digital data** into second **video** data having a second resolution less than the first resolution. The first and second video data represent first and second video programs, respectively. An overlay controller receives the first and second video data, and in response outputs a video frame signal simultaneously displaying at least portions of the first and second video programs. Hence, the apparatus uses a single MPEG **decoder** to obtain first and second video data representing first and second video programs, respectively, and an overlay controller to simultaneously display at least portions of the first and second video programs. The MPEG **decoder** performs the partial decompression of the second stream during idle intervals between frames from the first stream of compressed, digital data.

DETD FIGS. 3 and 5 are block diagrams illustrating different embodiments of the DET 52 of the present invention. The DET 52 portion of the set-top device in FIG. 3 includes an application processor 74, a digital video processor 75, and a peripheral interface 78. The DET 52 also includes non-volatile random access memory 80a, 80b for example electrically erasable programmable read only memory (EEPROM) or flash memory. Specifically, the DET 52 includes a RAM 80a for use by the application processor 74, and the digital video processor 75 comprises a **media processor** 76 and a RAM 80b. The RAM 80a and 80b each have a non-volatile portion for storing the operating system and software programming for the application processor 74 and the **media processor** 76, respectively. The software stored in the RAM 80a and 80b defines the basic functionality of the respective processors 74 and 76 in the DET 52. For example, the operating system stored in the RAM 80a controls how the application processor 74 interprets application programs. The operating system stored in the RAM 80a also includes the various driver routines permitting the application

processor to operate the other elements of the DET. The operating system stored in the RAM 80a and 80b also includes the basic or `resident` application under which the DET operates when not running a downloaded application. The resident application preferably emulates a cable television type program reception type user interface for the particular network to which the set-top connects.

DETD According to the embodiment of FIG. 3, the DET 52 operates as a distributed processing system, where the application processor 74 performs the background DET functions including control of DET operations, execution of downloaded applications, user interface functions, and generating upstream channel request and signaling messages in response to user inputs. The digital video processor 75 is a processing system dedicated to decompressing and decoding MPEG encoded data. The **media processor** 76 of FIG. 3 may be implemented as an enhanced microprocessor having multimedia-specific and digital signal processing instruction sets. The **media processor** 76 also includes high-bandwidth I/O to perform multimedia operations and MPEG decoding in real time. Hence, the RAM 80b stores operating system programming and instruction sets for optimized MPEG2 decoding and multimedia applications.

DETD As described above, the software controlling operation of the **media processor** in partially decompressing the secondary (PIP) transport stream is stored as a modified instruction set in the RAM 80b. The software may be downloaded by a technician via the interface 78 which can accommodate, for example, a PCMCIA card. Preferably, however, the software is downloaded from the network 10, for example as an enhanced service offered by the VIP 12. Specific details about downloading software into the DET 52 is disclosed in the above-incorporated application Ser. No. 08/498,265 (attorney docket 680-083D).

DETD Another variation of the disclosed embodiments involves fully decoding only a viewed portion of the primary program. Specifically, overlaying the secondary (PIP) program over the primary program causes a portion of the primary program of interest to be covered up by the PIP inset. Since the covered portion of the primary image is not visible to the viewer, it does not need to be fully decoded. Hence the **media processor** of FIG. 3 and the MPEG2 decoder 104 of FIG. 5 can be freed from the responsibility of fully decoding the covered portion of the primary video, so that significant processing power may be freed up for other tasks, such as decoding the PIP image.

CLM What is claimed is:

11. An apparatus comprising: a digital video processor decompressing a first stream of **compressed, digital data** representing a first **video** program into decompressed first video data having a first resolution, the digital video Processor outputting a video signal representing a frame of said first video data having a portion overlaid by decompressed second video data having a corresponding second resolution less than the first resolution; and an application processor partially decompressing a second stream of **compressed, digital data** representing a second **video** program into said second video data; wherein: the first and second streams carry MPEG-encoded video data having respective identifiers; the application processor comprises a microprocessor and a MPEG demultiplexer selectively routing the first and second streams to

the digital video processor and the microprocessor in response to the respective identifiers; and the digital video processor comprises: (1) an MPEG **decoder** decompressing the MPEG-encoded video data from the first stream, and (2) a graphics overlay controller receiving the first and second video data at first and second frame rates, respectively, and in response generating said video signal.

12. An apparatus comprising: a digital video processor decompressing a first stream of compressed, digital data representing a first video program into decompressed first video data having a first resolution, the digital video processor outputting a video signal representing a frame of said first video data having a portion overlaid by decompressed second video data having a corresponding second resolution less than the first resolution; and an application processor partially decompressing a second stream of compressed, digital data representing a second video program into said second video data; wherein the digital video processor comprises: a **media processor** decompressing said first stream of compressed, digital data; and a memory storing code executable by the **media processor** to control the decompressing of the first stream of compressed, digital data.

25. The apparatus of claim 24, wherein the digital video processor comprises: a digital **video decoder** decompressing the **compressed, digital data** from the first stream into said first video data; and a video overlay controller combining the first and second decompressed video data into said video signal.

28. The apparatus of claim 24, wherein the digital video processor comprises: a **media processor** decompressing the first stream of compressed, digital data; and a memory storing code executable by the **media processor** to control the decompressing of the first stream of compressed, digital data.

29. A digital entertainment terminal comprising: an application processor receiving multiplexed digital data carrying first and second streams of compressed, digital data representing first and second programs, respectively, the first and second streams having first and second identifiers, respectively, the application processor outputting the first stream of compressed digital data and a portion of the second stream of compressed, digital data in response to the respective first and second identifiers; and a **media processor** decompressing at least the first stream into first decompressed video data representing said first program, the **media processor** combining said first decompressed video data with second decompressed video data generated from said portion of the second stream and outputting the combined first and second video data as a video signal representing a video frame simultaneously displaying at least portions of said first and second video programs; wherein said portion of the second stream is partially decompressed into said second decompressed video data by one of said application **processor** and said **media processor**.

30. The terminal of claim 29, further comprising a buffer memory receiving from the application processor and storing the first stream and said portion of the second stream received from the **media processor**.

38. The terminal of claim 29, wherein the **media processor** partially decompresses a frame from said portion of the second stream between the decompression of two adjacent frames from said first stream.

42. An apparatus comprising: an MPEG **decoder** decompressing a first stream of **compressed, digital data** into first decompressed **video** data having a first resolution and partially decompressing a second stream of **compressed, digital data** into second decompressed **video** data having a second resolution less than the first resolution, the first and second decompressed video data representing first and second video programs, respectively; and an overlay controller receiving the first and second decompressed video data and in response outputting a video frame signal simultaneously displaying at least portions of the first and second video programs.

pn

L18 ANSWER 1 OF 1 USPATFULL
PI US 5847771 19981208

L16 ANSWER 1 OF 3 USPATFULL

DETD The video decoder device 6 is constructed so as to generate video soft data simultaneously in parallel with a plurality of channels 1 through k, and also the game decoder device 7 is similarly constructed so as to generate game soft data simultaneously in parallel with a plurality of channels 1 through m, so that the data files of the video/game softs successively designated by the control device 8 are intermittently read out in time division from the HDD 9 every predetermined blocks in accordance with the respective management information and stored respectively in the built-in internal memories (**DRAM**). The data read out of the respective **DRAM** is decoded and continuously outputted as a video/audio signal from a channel of a designated number.

DETD It is noted here that, as a capacity of each of the **DRAM** in the present embodiment, 256 kB.times.1 (Mbps), 256 kB.times.2 (Mbps), 256 kB.times.n (Mbps) where n is an integer, or other various capacity values may be appropriately used.

DETD The video **decoder** device 6 shown in FIG. 7 accommodates a plurality of MPEG **decoders** 64-1 through 64-k (represented by "64"), corresponding to the respective output channels (1 through k), serving as a data extending means for extending and thawing **digital data** of a **video** soft coded by **compression** in accordance with e.g. MPEG 2. In FIG. 7, the data intermittently read out in time division from a plurality of HDDs 9 every predetermined blocks is stored in DRAMs 62 via a SCSI controller 61 and read out via corresponding FIFOs 63 each having a capacity of e.g. 4 kB, and then **decoded** by the MPEG **decoders** 64 so as to be D/A converted, and thereafter outputted from the respective designated output channels and transferred to the switch 3. Herein, each unit within the video **decoder** device 6 is generally controlled by a DMA (direct memory access) microcomputer (CPU) 65.

DETD For a brief explanation, it is assumed a case where data corresponding to a video picture continual for several seconds is divided into e.g. four and stored in dispersion every blocks in the four HDDs 1 through 4, the data of the video soft A and soft B is alternately written by a pair of temporary storage semiconductor memories RAM 1A and RAM 1B, and when the transfer rate is e.g. 4 Mbps, a memory per one channel is 256 kB.times.4 (Mbps), and the **DRAM** writes data of 1 MB in amount corresponding to four blocks in the first writing, and thereafter, when the data of 256 kB is run out of in the writing operation, data of 256 kB is read out of the HDD, and thus the writing/reading operations are alternately repeated every 256 kB so that the reading is intermittently executed by time division every given blocks.

DETD In this case, the data read out from the HDDS 1-4 is transferred to each **DRAM** 62 shown in FIG. 7 and is temporarily stored in a predetermined region indicated by an upper half of the memory map shown in FIG. 6, for example, four 256 kB blocks (1 MB in total) corresponding to RAM 1A for channel 1.

DETD In this case, the data read out from the HDDS 1-4 is transferred to each

DRAM 62 in a similar manner to that of the soft And is temporarily stored in a predetermined region indicated by a lower half of the memory map shown in FIG. 6, for example, four 256 kB blocks (1 MB in total) corresponding to RAM 1B for channel 2.

DETD The data temporarily stored in each **DRAM** 62 is sequentially and consecutively read out every capacity of a corresponding FIFO 63 of e.g. 4 kB and transferred to a corresponding MPEG decoder 64.

DETD It is noted here that, in the present embodiment, 256 kB.times.1 (Mbps), 256 kB.times.2 (Mbps), or 256 kB.times.n (Mbps) where n is an integer and other various capacities can be appropriately used as the capacity of each **DRAM** as mentioned above.

DETD In this case, the data read out from the HDDS 1-4 is transferred to each **DRAM** 62 and is temporarily stored in a predetermined region indicated by a lower half of the memory map shown in FIG. 6, for example, four 256 kB blocks (1 MB in total) corresponding to RAM 1B.

DETD In this case, the data read out from the HDDS 1-4 is transferred to each **DRAM** 62 and is temporarily stored in a predetermined region indicated by an upper half of the memory map shown in FIG. 6, for example, four 256 kB blocks (1 MB in total) corresponding to RAM 2B.

DETD Next, when the control device 8 stores the input data of a video soft into HDDS 1-4, the input data is temporarily stored on **DRAM** represented by a memory map (256 kB.times.4) similar to the memory map shown in FIG. 6 and the data is sequentially transferred to the HDDS 1-4 in the order from that having prepared with the writing.

CLM What is claimed is:

7. The information processing device as claimed in claim 1, wherein the video/audio soft is a video soft having compression-coded data and said **decoder** means comprises a video **decoder** device for **decoding** the compression-coded video soft data, and wherein said video **decoder** device accommodates a plurality of MPEG **decoders** serving as data extending means for extending and thawing **digital data** of a **compression** -coded **video** soft, corresponding to the plural output channels.

8. The information processing device as claimed in claim 7, wherein said video decoder device accommodates a plurality of DRAMs for temporarily storing the digital data of the video/audio soft read out from said random-accessible large capacity storage means, a plurality of MPEG decoders arranged in parallel corresponding to said plural DRAMs for extending and restoring the read-out data, corresponding to the number of the channels of said video decoder device, and a pair of first-in data first-out memories arranged in parallel between said each **DRAM** and MPEG decoder for converting parallel data to serial data, whereby the data intermittently read out from said pair of DRAMs is continuously supplied to said MPEG decoder.

10. The information processing device as claimed in claim 9, wherein said game decoder device accommodates a plurality of DRAMs for temporarily storing the digital data of the game soft read out from said random-accessible large capacity storage means, a plurality of game decoder elements arranged in parallel corresponding to said plural DRAMs for extending and restoring the read-out data, corresponding to the number of the channels of said game decoder device, and bi-directional first-in data first-out memories arranged in parallel between said each **DRAM** and game decoder elements, whereby the data intermittently